PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-012819

(43)Date of publication of application : 14.01.2000

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(51)Int.Cl. H01L 27/146
H01L 27/148
H01L 27/14
H04N 5/335
H04N 9/07

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(54) SOLID-STATE IMAGE PICKUP ELEMENT

(57)Abstract:

PROBLEM TO BE SOLVED: To reduce dispersion in signals of pixels or a photoelectric converting section so as to improve the S/N ratio, by outputting signals of specific pixels, which are disposed in a checkered manner, from one of output terminals, and outputting signals of the other pixels from the other output terminal.

SOLUTION: Vertical signal lines 22a through 22d are respectively connected to pixels on odd-numbered rows of one of two adjacent pixel columns and to pixels on even-numbered rows on the other pixel column. And the vertical signal lines 22a through 22d have two horizontal signal lines. Namely, the vertical signal line 22a is connected to a pixel Px1-1 on the left on the first row, a pixel

Px2-2 on the right on the second row, and a pixel Px3-1 on the left on the third row. And then, the vertical signal lines 22a and 22c are connected to a horizontal signal line 2Va via column selecting transistors TH1 and TH3. The vertical signal lines 22b and 22d are connected to a horizontal signal line 27b via column selecting transistors TH2 and TH4.

LEGAL STATUS [Date of request for examination] 12.04.2005
[Date of sending the examiner's decision of rejection]
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]
[Date of final disposal for application]
[Patent number]
[Date of registration]
[Number of appeal against examiner's decision of rejection]
[Date of requesting appeal against examiner's decision of rejection]
[Date of extinction of right]

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CLAIMS

[Claim(s)]

[Claim 1] The solid state image sensor characterized by outputting the signal of the specific pixel which is the X-Y address type solid state image sensor equipped with two or more pixels arranged in the shape of a two-dimensional matrix, and two or more output terminals which output the signal of said pixel, and has been arranged in checkers among said pixels from one output terminal, and outputting the signal of other pixels from other output terminals.

[Claim 2] Two or more pixels arranged in the shape of a two-dimensional matrix, and two or more perpendicular signal lines to which said pixel was connected, It is the solid state image sensor equipped with two level signal lines to which said perpendicular signal line was connected through the switch. To each of said perpendicular signal line the inside of the pixel train of two adjacent trains -- the pixel of the oddth line of one pixel train -- and The solid state image sensor characterized by connecting the pixel of the eventh line of the pixel train of another side, connecting said odd-numbered perpendicular signal line to said one level signal line, and connecting said even-numbered perpendicular signal line to said level signal line of another side.

[Claim 3] Said pixel is a solid state image sensor according to claim 1 or 2 characterized by having the photo-electric-conversion section which generates the charge according to incident light, and the output section which outputs the signal according to said charge to a perpendicular signal line.

[Claim 4] Said pixel is a solid state image sensor according to claim 3 characterized by having further the transfer section which transmits said charge to said output section from said photo-electric-conversion section, and the control section which controls said output section.

[Claim 5] A solid state image sensor given in either of claim 1 to claims 4 characterized by the configuration of said protection-from-light field being the same by the pixel which the protection-from-light field was formed in said a part of pixel, and has been arranged at the oddth line, and the pixel arranged at the eventh line.

[Claim 6] A solid state image sensor given in either of claim 1 to claims 5 characterized by arranging the color filter of two or more classes corresponding to said pixel, and arranging said at least one kind of color filter in checkers.

[Claim 7] A solid state image sensor given in either of claim 1 to claims 5 characterized by arranging a green color filter in checkers and arranging the blue color filter with red line sequential corresponding to said other pixels corresponding to said pixel.

[Claim 8] The solid state image sensor characterized by being the CCD mold solid state image sensor equipped with two or more photo-electric-conversion sections arranged in the shape of a two-dimensional matrix, and two or more output terminals which output the signal of said photo-electric-conversion section, outputting the signal of the specific photo-electric-conversion section arranged in checkers among said photo-electric-conversion sections from one output terminal, and outputting the signal of other photo-electric-conversion sections from other output terminals.
[Claim 9] Two or more photo-electric-conversion sections arranged in the shape of a two-dimensional matrix, and two or more perpendicular transfer registers which transmit a signal charge in the direction of a reception train from said photo-electric-conversion section, It is the solid state image sensor equipped with two level transfer registers which transmit said signal charge to reception and a line writing direction from said perpendicular transfer register. Each of said perpendicular transfer register Among the photo-electric-conversion sections of two adjacent trains, the photo-electric-conversion section of the oddth line of one train, Reception and said one level transfer register said odd-numbered perpendicular transfer register to a signal charge for the photo-electric-conversion section of the eventh line of the train of another side to a signal charge And reception, Said level transfer register of another side is a solid state image sensor characterized by receiving a signal charge from said even-numbered perpendicular transfer register.
[Claim 10] A solid state image sensor given in either claim 8 characterized by the configuration of said protection-from-light field being the same in the photo-electric-conversion section which the protection-from-light field was formed in said a part of photo-electric-conversion section, and has been arranged at the oddth line, and the photo-electric-conversion section arranged at the eventh line, or claim 9.
[Claim 11] A solid state image sensor given in either of claim 8 to claims 10 characterized by arranging the color filter of two or more classes corresponding to said photo-electric-conversion section, and arranging said at least one kind of color filter in checkers.
[Claim 12] A solid state image sensor given in either of claim 8 to claims 10 characterized by arranging a green color filter in checkers and arranging the blue color filter with red line sequential corresponding to said other photo-electric-conversion sections corresponding to said photo-electric-conversion section.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the solid state image sensor of a juxtaposition output configuration in more detail about a solid state image sensor. The solid state image sensor of this invention is suitable to carry out a color image pick-up using the color filter arranged in checkers.

[0002]

[Description of the Prior Art] Various methods, such as a X-Y address type and a CCD mold, were proposed until now, and the solid state image sensor has resulted in utilization. First, the conventional X-Y address type solid state image sensor is explained with reference to a drawing. Drawing 23 is the circuit diagram showing the main configurations of the conventional X-Y address type solid state image sensor. Two or more pixel Px1-1-Px 3-4 by which the conventional X-Y address type solid state image sensor has been arranged in the shape of a two-dimensional matrix, The perpendicular signal lines 22a-22d to which the above-mentioned pixel was connected, and the level signal lines 27a and 27b to which the above-mentioned perpendicular signal line was connected through the train buffer amplifier 29a-29d, the clamp capacity Cc1-Cc4, and the train selection transistors TH1-TH4, the output-buffer amplifier 28a and 28b connected to the level signal line -- each -- it consists of a vertical-scanning circuit 7 which drives pixel Px1-1-Px 3-4, and a horizontal scanning circuit 8 which drives each train selection transistors TH1-TH4.

[0003] As illustrated, two or more arrangement of the level signal line is carried out. As

long as it is a solid state image sensor with few pixels, the level signal line of one sequence is sufficient. However, since the problem that sensibility and working speeds run short will arise if the number of pixels increases, it is more desirable to form two or more level signal lines, and to output to juxtaposition. The signal of pixel Px1-1-Px 3-4 is outputted to the perpendicular signal lines 22a-22d from the source (S) of JFET2. It is outputted to the level signal lines 27a and 27b via the train buffer amplifier 29a-29d, the clamp capacity Cc1-Cc4, and the train selection transistors TH1-TH4, and is outputted from output terminals 35a and 35b through the output-buffer amplifier 28a and 28b (Vout1, Vout2).

[0004] In addition, between the clamp capacity Cc1-Cc4 and the train selection transistors TH1-TH4, the clamp transistors Tc1-Tc4 are connected, and a fixed electrical potential difference (drawing 23 touch-down potential GND) can be impressed now to one electrode of clamp capacity. This is arranged in order to remove the noise produced in each pixel. Next, pixel structure is explained, referring to drawing 23 and drawing 24 . Drawing 24 is the top view of two or more pixels arranged in the shape of a matrix. Each pixel consists of the photodiode 1 which generates and accumulates the charge according to incident light, a junction field effect transistor (henceforth JFET) 2 which outputs the signal according to the above-mentioned charge from the source (S) by source follower actuation, the transfer gate 3 which transmits the above-mentioned charge to JFET2 from a photodiode 1, and the reset drain 4 which controls JFET2 and a reset gate 5. And each JFET2 is connected to the perpendicular signal lines 22a-22d for every train. In addition, the detail is indicated by JP,8-293591,A about unit pixel structure.

[0005] Next, the conventional CCD mold solid state image sensor is explained with reference to a drawing. Drawing 25 is the outline block diagram of the conventional CCD mold solid state image sensor. This component consists of two or more perpendicular transfer registers 220 which transmit a signal charge in the direction of a reception train from two or more photodiodes 210 arranged in the shape of a two-dimensional matrix, and a photodiode 210, level transfer registers 240a and 240b which transmit a signal charge to a reception line writing direction from the perpendicular transfer register 220, and charge detecting elements 250a and 250b.

[0006] The perpendicular transfer register 220 and the level transfer registers 240a and 240b are transmitted to the signal charge generated with the photodiode 210, it is changed into a voltage signal by the charge detecting elements 250a and 250b, and is outputted from output terminals 260a and 260b (Vout1, Vout2). Drawing 26 is the sectional view of the CCD mold solid state image sensor which met X1-X2 line of

drawing 25 . the N-type semiconductor substrate 200 top -- P type -- a well 201 is formed. a photodiode 210 -- this P type -- a well -- it is arranged in inside.

[0007] The signal charge generated with the photodiode 210 is accumulated in the N type charge storage field 211. The above-mentioned signal charge accumulated in the N type charge storage field 211 is first transmitted to the N type transfer channel field 221 of the perpendicular transfer register 220, and, subsequently to the direction of a train, a sequential transfer is carried out by actuation of the transfer electrode 224. By the way, when using a solid state image sensor for a color image pick-up, one color filter of red (R), green (G), and blue (B) is arranged on each photodiode of a solid state image sensor. Each pixel outputs the chrominance signal corresponding to the filter arranged at each pixel.

[0008] What has various arrays of each above-mentioned color filter of R, G, and B is proposed. Drawing 27 and drawing 28 show the typical color filter array arranged to a solid state image sensor in the case of a color image pick-up. green in the array shown in drawing 27 -- the color filter of (G) is arranged in the shape of a stripe every other train corresponding to a pixel, and the color filter of red (R) and blue (B) is arranged corresponding to the pixel of others which were left behind.

[0009] green in the array shown in drawing 28 -- the color filter of (G) is arranged in checkers and the color filter of red (R) and blue (B) is arranged line sequential corresponding to the pixel of others which were left behind (generally it is called a Bayer array). The color filter array by which the green (G) color filter has been arranged in the shape of a stripe every other train and which is shown in drawing 27 is suitable for the conventional solid state image sensor. The signal of the pixel equipped with the color filter of (G) goes via one level signal line (27a or 27b of drawing 23), or one level transfer register (240a or 240b of drawing 25). it serves as a principal component of a luminance signal -- green -- Since it is outputted from one output terminal (35a or 35b of drawing 23 , 260a or 260b of drawing 25), while latter signal processing becomes easy, it is for a fixed pattern noise to decrease and for the S/N ratio of a video signal to improve.

[0010]

[Problem(s) to be Solved by the Invention] however, the conventional solid state image sensor -- for example, green -- when the color filter of (G) was equipped with the color filter array shown in drawing 28 arranged in checkers, the fixed pattern noise occurred and there was a trouble that a S/N ratio fell. the signal of a pixel with which this has been arranged in checkers should pass two different paths (a level signal line or level transfer register) -- it is because it is outputted from two different output terminals.

[0011] It is made in view of the above-mentioned technical problem, and it is a juxtaposition output configuration, and signal dispersion of the pixel (or photo-electric-conversion section) arranged in checkers is reduced, and this invention aims at a S/N ratio offering a high solid state image sensor.

[0012]

[Means for Solving the Problem] Invention according to claim 1 is the X-Y address type solid state image sensor equipped with two or more pixels arranged in the shape of a two-dimensional matrix, and two or more output terminals which output the signal of said pixel, and is characterized by outputting the signal of the specific pixel arranged in checkers among said pixels from one output terminal, and outputting the signal of other pixels from other output terminals.

[0013] Since the signal of the pixel arranged in checkers is outputted from one output terminal, the fixed pattern noise of the signal outputted from the pixel arranged in checkers decreases, and its S/N ratio improves. It is suitable when it has the color filter of a checkered array especially. Two or more pixels by which invention according to claim 2 has been arranged in the shape of a two-dimensional matrix, It is the solid state image sensor equipped with two or more perpendicular signal lines to which said pixel was connected, and two level signal lines to which said perpendicular signal line was connected through the switch. To each of said perpendicular signal line the inside of the pixel train of two adjacent trains -- the pixel of the oddth line of one pixel train -- and It is characterized by connecting the pixel of the eventh line of the pixel train of another side, connecting said odd-numbered perpendicular signal line to said one level signal line, and connecting said even-numbered perpendicular signal line to said level signal line of another side.

[0014] Since the signal of the pixel arranged in checkers is outputted via one level signal line by this configuration, a fixed pattern noise decreases and its S/N ratio improves by it. It is suitable when it has the color filter of a checkered array especially. It is characterized by invention according to claim 3 having the photo-electric-conversion section in which said pixel generates the charge according to incident light, and the output section which outputs the signal according to said charge to a perpendicular signal line in the solid state image sensor indicated by claim 1 or 2. Moreover, in the solid state image sensor with which invention according to claim 4 was indicated by claim 3, said pixel is characterized by having further the transfer section which transmits said charge to said output section from said photo-electric-conversion section, and the control section which controls said output section.

[0015] It becomes possible to output not the charge itself produced in incident light by these configurations but the signal (for example, the signal by which charge magnification was carried out and the signal by which current amplification was carried out) changed by this charge. Invention according to claim 5 is a solid state image sensor given in either of claim 1 to claims 4, is the pixel which the protection-from-light field was formed in said a part of pixel, and has been arranged at the oddth line, and the pixel arranged at the eventh line, and is characterized by the configuration of said protection-from-light field being the same.

[0016] By this configuration, the light-receiving property of each pixel becomes the same, a fixed pattern noise decreases, and a S/N ratio improves. Invention according to claim 6 is the solid state image sensor indicated by either of claim 1 to claims 5, and is characterized by arranging the color filter of two or more classes corresponding to said pixel, and arranging said at least one kind of color filter in checkers.

[0017] When carrying out a color image pick-up, a color filter is arranged at each pixel of a solid state image sensor. Generally a color filter has the class of two or more colors. As for invention of claim 7, the color filter of Isshiki is arranged in checkers at least among two or more of these color filters. For this reason, a fixed pattern noise decreases and the S/N ratio of the signal corresponding to this color improves. Invention according to claim 7 is the solid state image sensor indicated by either of claim 1 to claims 5, and is characterized by arranging a green color filter in checkers and arranging the blue color filter with red line sequential corresponding to said other pixels corresponding to said pixel. This claim shows the class of concrete color filter.

[0018] Two or more photo-electric-conversion sections by which invention according to claim 8 has been arranged in the shape of a two-dimensional matrix, It is the CCD mold solid state image sensor equipped with two or more output terminals which output the signal of said photo-electric-conversion section. The signal of the specific photo-electric-conversion section arranged in checkers among said photo-electric-conversion sections is characterized by being outputted from one output terminal and outputting the signal of other photo-electric-conversion sections from other output terminals.

[0019] Since the signal of the photo-electric-conversion section arranged in checkers is outputted from one output terminal, the fixed pattern noise of the signal outputted from the photo-electric-conversion section arranged in checkers decreases, and its S/N ratio improves. It is suitable when it has the color filter of a checkered array especially. Two or more photo-electric-conversion sections by which invention according to claim 9 has been arranged in the shape of a two-dimensional matrix, Two or more perpendicular

transfer registers which transmit a signal charge in the direction of a reception train from said photo-electric-conversion section, It is the solid state image sensor equipped with two level transfer registers which transmit said signal charge to reception and a line writing direction from said perpendicular transfer register. Each of said perpendicular transfer register Among the photo-electric-conversion sections of two adjacent trains, the photo-electric-conversion section of the oddth line of one train, Reception and said one level transfer register said odd-numbered perpendicular transfer register to a signal charge for the photo-electric-conversion section of the eventh line of the train of another side to a signal charge And reception, Said level transfer register of another side is characterized by receiving a signal charge from said even-numbered perpendicular transfer register.

[0020] The signal of the photo-electric-conversion section arranged in checkers is outputted via one level transfer register. For this reason, a fixed pattern noise decreases and a S/N ratio improves. It is suitable especially when it has the color filter of a checkered array. Invention according to claim 10 is a solid state image sensor given in either claim 8 or claim 9, is the photo-electric-conversion section which the protection-from-light field was formed in said a part of photo-electric-conversion section, and has been arranged at the oddth line, and the photo-electric-conversion section arranged at the eventh line, and is characterized by the configuration of said protection-from-light field being the same.

[0021] By this configuration, the light-receiving property of each photo-electric-conversion section becomes the same, a fixed pattern noise decreases, and a S/N ratio improves. Invention according to claim 11 is the solid state image sensor indicated by either of claim 8 to claims 10, and is characterized by arranging the color filter of two or more classes corresponding to said photo-electric-conversion section, and arranging said at least one kind of color filter in checkers.

[0022] When carrying out a color image pick-up, a color filter is arranged at each photo-electric-conversion section of a solid state image sensor. Generally a color filter has the class of two or more colors. As for invention of claim 11, the color filter of Isshiki is arranged in checkers at least among two or more of these color filters. For this reason, a fixed pattern noise decreases and the S/N ratio of the signal corresponding to this color improves.

[0023] Invention according to claim 12 is the solid state image sensor indicated by either of claim 8 to claims 10, and is characterized by arranging a green color filter in checkers and arranging the blue color filter with red line sequential corresponding to said other photo-electric-conversion sections corresponding to said

photo-electric-conversion section. This claim shows the class of concrete color filter.
[0024]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained with reference to a drawing. In addition, the same sign's being the same or the explanation which shows a considerable part and overlaps is omitted among each drawing.
[Operation gestalt 1] Drawing 1 is the circuit diagram showing the outline of the solid state image sensor by the operation gestalt 1 of this invention.
[0025] Two or more pixel Px1-1-Px 3-4 which the solid state image sensor by the operation gestalt 1 is a X-Y address type solid state image sensor, and has been arranged in the shape of a two-dimensional matrix, The perpendicular signal lines 22a-22d to which the pixel of two adjacent trains was connected by turns at intervals of a pixel, The level signal lines 27a and 27b to which the perpendicular signal lines 22a-22d were connected by turns through the train selection transistors TH1-TH4, the output terminals 35a and 35b prepared in the level signal lines 27a and 27b -- each -- it consists of a vertical-scanning circuit 7 which drives pixel Px1-1-Px 3-4, and a horizontal scanning circuit 8 which drives each train selection transistors TH1-TH4.
[0026] In addition, as for the pixel of the actual solid state image sensor of this operation gestalt, a line writing direction and the direction of a train are arranged 100 or more. Drawing 1 (each circuit diagram showing another operation gestalt in a list) shows the part for convenience. Here, although the number of pixels was performed above, this invention is not restricted to this. For example, according to an application, a pixel may arrange a line writing direction and the direction of a train 1000 or more.
[0027] The pixel of the oddth line of one pixel train and the pixel of the eventh line of the pixel train of another side are connected among the pixel trains of two trains which adjoin perpendicular signal lines [22a-22d] each, and the solid state image sensor of the operation gestalt 1 has two level signal lines. Namely, the party eye went in the drawing, a left-hand side pixel (Px 1-1) and the second line connect a right-hand side pixel (Px 2-2), and, as for perpendicular signal-line 22a, the third line has connected the left-hand side pixel (Px 3-1). And the perpendicular signal lines 22a and 22c are connected to one level signal-line 27a through the train selection transistors TH1 and TH3. The perpendicular signal lines 22b and 22d are connected to level signal-line 27b of another side through the train selection transistors TH2 and TH4.
[0028] Thus, the signal which will be outputted from the pixel (pixel arranged in checkers) of Px 1-1, Px 1-3, Px 2-2, Px 2-4, Px 3-1, and Px 3-3 if it connects becomes possible [outputting to the exterior of a solid state image sensor via the same level

signal line]. Since it goes via the same level signal line, a fixed pattern noise is reduced. Moreover, a green (G) color filter is prepared in checkers, and is arranged on a corresponding pixel (Px 1-1, Px 1-3, Px 2-2, Px 2-4, Px 3-1, Px 3-3). A blue (B) color filter is arranged with red (R) line sequential at the pixel of others which were left behind (Bayer array).

[0029] thus, green, when a color filter is arranged -- the signal of (G) is outputted from output terminal 35a via the same level signal-line 27a. Moreover, the signal of red (R) and blue (B) is outputted from output terminal 35b via level signal-line 27b of another side. as mentioned above, the solid state image sensor of the operation gestalt 1 has been arranged in checkers -- green -- the signal of the pixel equipped with the color filter of (G) is outputted from one output terminal 35a via one level signal-line 27a. Therefore, while latter signal processing becomes easy compared with the conventional X-Y address type solid state image sensor, a fixed pattern noise decreases and a S/N ratio improves.

[Operation gestalt 2] Drawing 2 is the circuit diagram showing the outline of the solid state image sensor by the operation gestalt 2 of this invention.

[0030] The solid state image sensor by the operation gestalt 2 is a X-Y address type solid state image sensor, and consists of line selection transistors 42 which transmit the charge of the photodiode 41 with which one pixel (for example, Px 1-1) generates and accumulates the charge according to incident light, and a photodiode 41 to perpendicular signal-line 22a. Each pixel covers fields other than photodiode 41 with the film (light-shielding film) which has protection-from-light nature, is the pixel of the oddth line, and a pixel of the eventh line, and is good also as the same in the configuration of a protection-from-light field. If it does in this way, the location of the area of a light sensing portion, a configuration, and an optical center of gravity will become the same [the pixel of the oddth line, and the pixel of the eventh line], and the variation in a light-receiving property will be reduced. Other configurations are the same as that of the solid state image sensor of the operation gestalt 1.

[0031] moreover -- each -- the photodiode 41 of pixel Px1-1-Px 3-4 -- corresponding -- the solid state image sensor of the operation gestalt 1 -- the same -- red (R) -- green -- each color filter of (G) and blue (B) is arranged. for this reason, green -- and the signal of (G) is outputted from output terminal 35a via level signal-line 27a. [while] Moreover, the signal of red (R) and blue (B) is outputted from output terminal 35b via level signal-line 27b of another side.

[0032] Therefore, like the solid state image sensor of the operation gestalt 1, while latter signal processing becomes easy, a fixed pattern noise decreases and the S/N ratio of the

solid state image sensor of the operation gestalt 2 improves.

[Operation gestalt 3] Drawing 3 is the circuit diagram showing the outline of the solid state image sensor by the operation gestalt 3 of this invention.

[0033] The photodiode 51 with which the solid state image sensor by the operation gestalt 3 is a X-Y address type solid state image sensor, and one pixel (for example, Px 1-1) generates and accumulates the charge according to incident light, The transistor 52 which detects the potential of a photodiode 51 and is outputted from the source (S) by source follower actuation, It consists of reset transistors 53 which initialize the line selection transistor 54 which connects the source (S) of a transistor 52, and perpendicular signal-line 22a, and a photodiode 51 and a transistor 52. In addition, the potential of a photodiode 51 is changed according to the amount of the accumulated charge.

[0034] The signal of pixel Px1-1-Px 3-4 is outputted to the perpendicular signal lines 22a-22d through the line selection transistor 54 from the source (S) of a transistor 52. It is outputted to the level signal lines 27a and 27b via the train buffer amplifier 29a-29d, the clamp capacity Cc1-Cc4, and the train selection transistors TH1-TH4. It is outputted from output terminals 35a and 35b through the output-buffer amplifier 28a and 28b (Vout1, Vout2).

[0035] By the way, each pixel and perpendicular signal lines [22a-22d] connection relation is the same as that of the operation gestalt 1, and the pixel of two trains which adjoin perpendicular signal lines [22a-22d] each is connected by turns at intervals of a pixel. Moreover, it connects with the clamp transistors TC1-TC4 through the train buffer amplifier 29a-29d and the clamp capacity Cc1-Cc4, and the perpendicular signal lines 22a-22d are further connected to the level signal lines 27a and 27b by turns through the train selection transistors TH1-TH4 while connecting with the perpendicular load-carrying capacity Cv1-Cv4.

[0036] Therefore, like the solid state image sensor of the operation gestalt 1, while latter signal processing becomes easy, a fixed pattern noise decreases and the S/N ratio of the solid state image sensor of the operation gestalt 3 improves. Moreover, the solid state image sensor of the operation gestalt 3 covers fields other than photodiode 51 of each pixel with a light-shielding film like the solid state image sensor of the operation gestalt 2, and even if it is the same in the configuration of a protection-from-light field at the pixel of the oddth line, and the pixel of the eventh line, it is good.

[0037] Moreover, since the band of source follower actuation of a transistor 52 is restricted by the perpendicular load-carrying capacity Cv1-Cv4, a noise decreases further. That is, the solid state image sensor of this operation gestalt carries out

subtraction processing of a source follower output when a photodiode 51 accumulates a signal charge, and the source follower output after resetting the signal charge of a photodiode 51 through the clamp capacity Cc1-Cc4. By this processing, the fixed pattern noise by dispersion in the threshold electrical potential difference of a transistor 52, the 1/f noise at the time of source follower actuation, and the fixed pattern noise by dispersion in train buffer amplifier [29a-29d] offset voltage decrease, and its S/N ratio improves further.

[Operation gestalt 4] Drawing 4 is the circuit diagram showing the configuration of the solid state image sensor by the operation gestalt 4 of this invention. The solid state image sensor by the operation gestalt 4 is a X-Y address type solid state image sensor, and the pixel configuration differs from the solid state image sensor of the operation gestalt 3. Moreover, in connection with it, wiring for a scan connected to a vertical-scanning circuit or it differs.

[0038] One pixel 1-3 of the solid state image sensor by the operation gestalt 4, for example, Px, consists of the photodiode 1 which generates and accumulates the charge according to incident light, a junction field effect transistor (henceforth JFET) 2 which outputs the signal according to the above-mentioned charge from Source S by source follower actuation, the transfer gate 3 which transmits the above-mentioned charge to JFET2 from a photodiode 1, and the reset drain 4 which controls JFET2 and a reset gate 5.

[0039] Other configurations are almost the same as that of the solid state image sensor of the operation gestalt 3. Drawing 5 is the top view of two or more pixels of the solid state image sensor concerning this operation gestalt. Each pixel consists of a photodiode 1, JFET2, the transfer gate 3, a reset drain 4, and a reset gate 5. And structure has reversed the pixel arranged at the oddth line, and the pixel arranged at the eventh line, and JFET2 which is the pixel of two adjacent trains is connected to the perpendicular signal line 22 (it corresponds to the perpendicular signal lines 22a-22d of drawing 4) by turns at intervals of a pixel.

[0040] The transfer gate 3 is connected to the transfer gate wiring 20 (it corresponds to the transfer gate wiring 20a-20c of drawing 4), and the reset gate 5 is connected to the reset gate wiring 21 (it corresponds to the reset gate wiring 21a-21c of drawing 4), respectively. The reset drain 4 is connected to the reset drain wiring 24 (it corresponds to the reset drain wiring 24a-24c of drawing 4) through the junction wiring 23 (refer to drawing 7).

[0041] Fields other than photodiode 1 of each pixel are shaded with the reset drain wiring 24 and the perpendicular signal line 22 which were formed with the ingredient

which has protection-from-light nature, such as aluminum. By this, the pixel of the oddth line and the pixel of the eventh line become the same [the location of the area of a light-receiving field, a configuration, and an optical center of gravity]. For this reason, a fixed pattern noise decreases further and a S/N ratio improves further.

[0042] In the solid state image sensor of this operation gestalt, wiring for a scan and a perpendicular signal line were made to serve a double purpose as a light-shielding film as mentioned above. Therefore, a production process decreases rather than it arranges the film of dedication as a light-shielding film. For this reason, the yield improves and a manufacturing cost is reduced. However, conversely, the aluminum film may be only formed in light-shielding films, and patterning may be carried out so that a light-receiving field may carry out opening. If it does in this way, there will be no need of using wiring also [light-shielding film], and the degree of freedom of a wiring design will improve.

[0043] Moreover, the solid state image sensor of this operation gestalt arranges each color filter of red (R), green (G), and blue (B) to the photodiode 1 of each pixel as well as the solid state image sensor concerning the operation gestalt 1. for this reason, green -- and the signal of (G) is outputted from output terminal 35a via level signal-line 27a. [while] For this reason, while latter signal processing becomes easy, a fixed pattern noise decreases and a S/N ratio improves.

[0044] Hereafter, with reference to drawing 6 - drawing 9 , the pixel structure of the solid state image sensor of the operation gestalt 4 is further explained to a detail. The top view of one pixel of the solid state image sensor which drawing 6 requires for this operation gestalt, the sectional view where drawing 7 met X1-X2 line of drawing 6 , the sectional view where drawing 8 met Y1-Y2 line of drawing 6 , and drawing 9 are the sectional views which met Y3-Y4 line of drawing 6 . In addition, the color filter is omitted in these drawings.

[0045] the N type formed on the P-type semiconductor substrate 10 as a photodiode 1 was shown in drawing 8 and drawing 9 -- a well -- it is constituted by a field 11, the P type charge storage field 12, and the high-concentration N-type semiconductor field 13. Thereby, the photodiode of a flush type is formed with the vertical mold overflow drain structure of a NPNP mold. That is, the structure to which the photodiode (N, P, N) of an embedding mold and vertical mold overflow drain structure (P, N, P) were joined is formed. The configuration of the photodiode of a flush type has the dark current, an after-image, a reset noise, a blooming, and the effectiveness of reducing a smear, with vertical mold overflow drain structure.

[0046] JFET2 consists of the N type source field 14, a P type gate field 15, an N type

drain field 16, and an N type channel field 17, as shown in drawing 7 and drawing 8 . The transfer gate 3 is formed through the insulator layer 33 on the border area of a photodiode 1 and JFET2, as shown in drawing 8 . the reset drain 4 is shown in drawing 7 and drawing 9 -- as -- N type -- a well -- it consists of P type charge discharge fields 18 in a field 11. The reset gate 5 is formed through the insulator layer 33 on the border area of JFET2 and the reset drain 4, as shown in drawing 7 .

[0047] as mentioned above, the solid state image sensor of the operation gestalt 4 has been arranged in checkers -- green -- the signal of the pixel equipped with the color filter of (G) is outputted from one output terminal 35a via one level signal-line 27a and one output-buffer amplifier 28a. Therefore, like the solid state image sensor of the operation gestalt 1, while latter signal processing becomes easy, a fixed pattern noise decreases and a S/N ratio improves.

[0048] Moreover, fields other than photodiode 1 of each pixel are shaded with the reset drain wiring 24 and the perpendicular signal line 22, the solid state image sensors of the operation gestalt 4 are the pixel of the oddth line, and the pixel of the eventh line, since the configuration of a protection-from-light field is the same, a fixed pattern noise decreases and its S/N ratio improves further. Moreover, the dark current, an after-image, a reset noise and a blooming, and a smear are reduced for vertical mold overflow drain structure and the photodiode structure of a flush type. Furthermore, since the band of source follower actuation of JFET2 is restricted by the perpendicular load-carrying capacity Cv1-Cv4, a noise decreases, and a S/N ratio improves further.

[0049] Furthermore, the source follower output of JFET2 after initialization (before a signal-charge transfer), By carrying out subtraction processing (the so-called correlation duplex sampling processing) of the source follower output of JFET2 after a signal-charge transfer from a photodiode 1 through the clamp capacity Cc1-Cc4 to JFET2 The fixed pattern noise by dispersion in the threshold electrical potential difference of JFET2, the 1/f noise at the time of source follower actuation, The reset noise generated when the fixed pattern noise by dispersion in the offset voltage of the train buffer amplifier 29a-29b not only decreases, but JFET2 is initialized through a reset gate 5 is also reduced. For this reason, a S/N ratio improves further.

[Operation gestalt 5] Drawing 10 is the circuit diagram showing the configuration of the solid state image sensor by the operation gestalt 5 of this invention, and drawing 11 is the top view of two or more pixels arranged in the shape of [the] a matrix.

[0050] The solid state image sensor by the operation gestalt 5 is a X-Y address type solid state image sensor, and the pixel configuration differs from the solid state image sensor of the operation gestalt 4. Other configurations are the same as that of the solid

state image sensor of the operation gestalt 4, and the explanation is omitted. Here, the pixel structure of the solid state image sensor applied to this operation gestalt with reference to a drawing is explained. Drawing 12 is the top view of one pixel of the solid state image sensor concerning this operation gestalt, and the sectional view where drawing 13 met X1-X2 line of drawing 12 , the sectional view where drawing 14 met Y1-Y2 line of drawing 12 , and drawing 15 are the sectional views which met Y3-Y4 line of drawing 12 .

[0051] One pixel consists of two overflow control field 6a [two] per a photodiode 1, JFET2, the transfer gate 3, and 4 or 1 pixel of reset drains per 5 or 1 pixel of reset gates (refer to drawing 12). The above-mentioned photodiode 1, JFET2, the reset drain 4, and overflow control field 6a are prepared into the N-type semiconductor layer 101 on the high-concentration N-type semiconductor substrate 100. The transfer gate 3 and a reset gate 5 are formed through an insulator layer 33 on the N-type semiconductor layer 101.

[0052] A photodiode 1 is constituted by the N-type semiconductor layer 101 formed on the high-concentration N-type semiconductor substrate 100, the P type charge storage field 12, and the high-concentration N-type semiconductor field 13 as shown in drawing 14 and drawing 15 . That is, the embedded photodiode of an NPN mold is formed. JFET2 is formed into the N-type semiconductor layer 101 on the high-concentration N-type semiconductor substrate 100, as shown in drawing 13 and drawing 14 . Therefore, the drain field 16 of JFET2 is electrically connected with the high-concentration N-type semiconductor substrate 100 through the N-type semiconductor layer 101. Therefore, the drain electrical potential difference VD (refer to drawing 10) can be supplied to the drain field 16 of JFET2 via the high-concentration N-type semiconductor substrate 100. Since the high-concentration N-type semiconductor substrate 100 has small electric resistance, even if it arranges many pixels, it can oppress fluctuation of the drain electrical potential difference for every JFET.

[0053] This drain electrical potential difference VD forms contact in the perimeter of a pixel field (field where two or more arrangement of the pixel was carried out at the shape of a matrix), may be supplied via the semi-conductor substrate 100, or may form and supply contact to the rear face of the semi-conductor substrate 100. The P type charge discharge field 18 of the reset drain 4 is connected to the reset drain wiring 24 through the junction wiring 23, as shown in drawing 13 .

[0054] The reset gate 5 is formed at two rate per pixel, as shown in drawing 12 and drawing 13 . Therefore, the P type gate field 15 of JFET2 and the P type charge discharge field 18 of the reset drain 4 are connected to the line writing direction through

the reset gate 5 at the serial. Overflow control field 6a is arranged in the border area of a photodiode 1 and the reset drain 4 for overflow. If the superfluous quantity of light carries out incidence to a photodiode and the generated charge generally exceeds the capacity (the maximum charge accumulated dose) of a photodiode, a superfluous charge will overflow and a blooming will be produced. Overflow control field 6a discharges this superfluous charge to the reset drain 4, and prevents a blooming. Overflow control field 6a is arranged between a photodiode 1 and two reset drains 4 which adjoin this, as shown in drawing 12 , drawing 14 , and drawing 15 . That is, overflow control field 6a is arranged at two rate per pixel in the border area of a photodiode 1 and the reset drain 4.

[0055] Thus, the pixel structure of the solid state image sensor of this operation gestalt is constituted by the embedded photodiode 1 of an NPN mold, overflow control field 6a, and the reset drain 4, and, thereby, an embedding mold photodiode and horizontal-type overflow drain structure are formed. Here, it returns and explains to drawing 10 and 11. As for the solid state image sensor of this operation gestalt, the above-mentioned pixel is arranged in the shape of a matrix. By the way, the gate field and the reset drain 4 of JFET2 of each pixel which have been arranged at the line writing direction (it sets to drawing 10 and 11 and is a longitudinal direction) are altogether connected to the serial through the reset gate 5. By this configuration, the defect by open circuit of reset drain wiring is reduced. That is, in a certain pixel, even if the defect in the release mode in which connection between the reset drain 4 and the reset drain wiring 24, 24a-24c becomes imperfect occurs, it connects with JFET2 of the above-mentioned pixel from the reset drain 4 of other pixels. For this reason, possibility of being disconnected becomes very small.

[0056] Other configurations are the same as that of the solid state image sensor of the operation gestalt 4. For this reason, a fixed pattern noise reduces the solid state image sensor of the operation gestalt 5 like the solid state image sensor of the operation gestalt 4, and its S/N ratio improves. Moreover, even if the defect in the release mode in which connection with the reset drain 4 becomes imperfect occurs, since JFET2 is controllable, the manufacture yield of the solid state image sensor of the operation gestalt 5 improves.

[0057] Moreover, since the drain electrical potential difference VD is supplied to the drain field 16 of JFET2 via the high-concentration (low resistance) N-type semiconductor substrate 100, the fluctuation for every pixel of a drain electrical potential difference decreases, and a fixed pattern noise decreases. Moreover, the P type charge storage field 12 of a photodiode 1 and the N-type semiconductor substrate 100 of an opposite conductivity type are used. For this reason, the signal charge (in this case,

electron hole) generated in photodiode 1 deep part is also accumulated in a photodiode 1, and its sensibility improves.

[Operation gestalt 6] Drawing 16 is the top view of two or more pixels arranged in the shape of [of the solid state image sensor concerning the operation gestalt 6 of this invention] a matrix.

[0058] The solid state image sensor of the operation gestalt 6 is a X-Y address type solid state image sensor, and the relative physical relationship of the photodiode 1 arranged at the pixel, JFET2, the transfer gate 3, the reset drain 4, a reset gate 5, and overflow control field 6a and the configuration of the wiring section differ from the solid state image sensor of the operation gestalt 5. That is, the reset gate 5 in the protection-from-light field to which the solid state image sensor of the operation gestalt 6 was covered with the reset drain wiring 24, the perpendicular signal line 22, and the junction wiring 23 serve as the configuration and arrangement of the oddth line of the eventh line same at a pixel and a pixel. Therefore, it is the same to the cross-section configuration of the whole pixel not only including the superficial configuration of a protection-from-light field but wiring and an insulator layer. For this reason, dispersion in a light-receiving property decreases further.

[0059] The configuration of others including a circuit diagram is the same as that of the solid state image sensor of the operation gestalt 5 (refer to drawing 10). Therefore, a fixed pattern noise reduces the solid state image sensor of the operation gestalt 6 like the solid state image sensor of the operation gestalt 5, and a S/N ratio, the yield, and its sensibility improve. Moreover, the solid state image sensors of the operation gestalt 6 are the pixel of the eventh line, and the pixel of the oddth line, since the cross-section configuration of wiring or an insulator layer also becomes the same, a fixed pattern noise decreases and its S/N ratio improves further.

[Operation gestalt 7] Drawing 17 is the circuit diagram showing the outline of the solid state image sensor by the operation gestalt 7 of this invention. The solid state image sensor of the operation gestalt 7 is a X-Y address type solid state image sensor, and the configuration from the perpendicular signal lines 22a-22d to output terminals 35a and 35b differs from the solid state image sensor of the operation gestalt 5.

[0060] The perpendicular signal lines 22a-22d to which the pixel of two adjacent trains was connected by turns at intervals of a pixel are connected to the level signal lines 27a or 27c (signal output line) through the train selection transistors THS1-THS4 while connecting with the signal output storage capacitance CS1-CS4 through the transistors TS1-TS4 for a signal output transfer. Furthermore, the perpendicular signal lines 22a-22d are connected to the level signal lines 27b or 27d (dark output line) through the

train selection transistors THD1-THD4 while connecting with the dark output storage capacitance CD1-CD4 through the transistors TD1-TD4 for a dark output transfer. That is, the perpendicular signal lines 22a-22d are connected to the level signal line (signal output line 27c, 27d of dark output lines) of the group of 1 set of level signal lines (signal output line 27a, dark output line 27b), and others by turns.

[0061] The level signal lines 27a-27d are connected to differential amplifier 34a and 34b through the output-buffer amplifier 28a-28d. Thus, four level signal lines 27a-27d are arranged. However, the level signal lines 27a and 27b and the level signal lines 27c and 27d are a pair. That is, 2 sets (two) of level signal lines are arranged.

[0062] For example, a pixel Px 1-1, Px 2-2, and Px 3-1 are connected to perpendicular signal-line 22a. The path (namely, TS1-CS1-THS1-27a-28a) which accumulates and outputs the lightwave signal with which perpendicular signal-line 22a contains a noise (dark output), and the path (namely, TD1-CD1-THD1-27b-28b) which accumulates a noise (dark output) and is outputted are connected. The output-buffer amplifier 28a and 28b connected to each path is connected to differential-amplifier 34a. And subtraction processing is carried out and the signal outputted from each path is outputted from one output terminal 35a.

[0063] On the other hand, a pixel Px 1-2, Px 2-3, and Px 3-2 are connected to perpendicular signal-line 22b. And the path (namely, TS2-CS2-THS2-27c-28c) which accumulates and outputs the lightwave signal with which perpendicular signal-line 22b includes a dark output, and the path (namely, two to 27 d TD2-CD2-THD to 28 d) which accumulates a dark output and is outputted are connected. The output-buffer amplifier 28c and 28d connected to each path is connected to differential-amplifier 34b, subtraction processing is carried out and the signal outputted from each path is outputted from output terminal 35b of another side.

[0064] Here, actuation of the solid state image sensor of this operation gestalt is explained briefly. First, the source follower output (dark output) of JFET2 after initialization (before a signal-charge transfer) is accumulated in CD1-CD4. Next, it is the source follower output of JFET2 after a signal-charge transfer (signal output.) to JFET2 from a photodiode 1. a dark output component -- containing -- it accumulates in CS1-CS4. Subsequently, subtraction processing of a signal output and the dark output is carried out with differential amplifier 34a and 34b through the train selection transistors THS1-THS4, THD1-THD4, the level signal lines 27a-27d, and the output-buffer amplifier 28a-28d. By this actuation, the so-called correlation duplex sampling processing is made, and the true signal output from which the dark output component was deducted is obtained.

[0065] In addition, "the fixed pattern noise by dispersion in the threshold electrical potential difference of JFET2", "the fixed pattern noise by dispersion in train buffer amplifier [29a-29d] offset voltage", "the 1/f noise at the time of source follower actuation", and "the reset noise when initializing JFET2" are contained in the dark output indicated here. In addition, in order to avoid the effect of an external noise, as for the output-buffer amplifier 28a-28d, it is desirable to prepare in the interior of a solid state image sensor. On the other hand, differential Anh 34a and 34b may prepare in the exterior of a solid state image sensor.

[0066] moreover, green -- green, since the color filter of (G) is arranged on the pixel (Px 1-1, Px 1-3, Px 2-2, Px 2-4, Px 3-1, Px 3-3) which prepares in checkers and corresponds -- and the signal of (G) is outputted from output terminal 35a via the level signal lines 27a and 27b of a group. [while] Moreover, the signal of red (R) and blue (B) is outputted from output terminal 35b via the level signal lines 27c and 27d of the group of another side. For this reason, while latter signal processing becomes easy, a fixed pattern noise decreases and a S/N ratio improves.

[Operation gestalt 8] Drawing 18 is the block diagram showing the outline of the solid state image sensor by the operation gestalt 8 of this invention. The solid state image sensor by the operation gestalt 8 is a CCD mold solid state image sensor, and has two or more perpendicular transfer registers 220 which transmit a signal charge in reception and the direction of a train by turns alternately, two level transfer registers 240a and 240b which transmit a signal charge to a reception line writing direction from the perpendicular transfer register 220, and charge detecting elements 250a and 250b from two or more photodiodes 210 arranged in the shape of a two-dimensional matrix, and the photodiode 210 of two adjacent trains.

[0067] It distributes among the level transfer registers 240a and 240b, a transfer electrode (not shown) is arranged, and a signal charge is transmitted with this electrode to either level transfer register 240a or level transfer register 240b. phiV1 to phiV3 is a pulse voltage impressed to the transfer electrode (after-mentioned) of the perpendicular transfer register 220, and phiHG is a pulse voltage impressed to the distribution transfer electrode between level transfer register 240a and 240b.

[0068] Moreover, the color filter of red (R), green (G), and blue (B) is arranged in the same array as the operation gestalt 1 at each photodiode 210. The perpendicular transfer register 220 and the level transfer registers 240a and 240b are transmitted to the signal charge generated with the photodiode 210, it is changed into a voltage signal by the charge detecting elements 250a and 250b, and is outputted from output terminals 260a and 260b (Vout1, Vout2).

[0069] Thus, the solid state image sensor of the operation gestalt 8 has received the signal charge from the photodiode 210 of 2 of the perpendicular transfer register 220 which adjoin each other, respectively trains by turns alternately. Namely, a party eye goes in a drawing, a left-hand side pixel and the second line receive a right-hand side pixel, and, as for each perpendicular transfer register, the third line receives a charge signal from a left-hand side pixel.

[0070] And the signal charge outputted from each of the perpendicular transfer register 220 is transmitted to the level signal registers 240a and 240b by turns. Thus, if it connects, the signal charge outputted from the pixel arranged in checkers will be outputted to the exterior of a solid state image sensor via the same level transfer register. Since it goes via the same level transfer register, a fixed pattern noise is reduced.

[0071] Hereafter, with reference to drawing 19 - drawing 21 , the pixel structure of the solid state image sensor of the operation gestalt 4 is further explained to a detail. The top view of the field 300 where drawing 19 was surrounded with the broken line of drawing 18 , the sectional view where drawing 20 met X1-X2 line of drawing 19 , and drawing 21 are the sectional views which met X3-X4 line of drawing 19 . In addition, the color filter is omitted in this drawing. the P type formed on the N-type semiconductor substrate 200 as a photodiode 210 was shown in drawing 20 -- a well -- it is constituted by a field 201, the N type charge storage field 211, and the high-concentration P-type semiconductor field 212. Thereby, the photodiode of a flush type is formed with the vertical mold overflow drain structure of a PNPN mold. That is, the structure to which an embedding photodiode (P, N, P) and vertical mold overflow drain structure (N, P, N) were joined is formed. It embeds with vertical mold overflow drain structure, and the configuration of the photodiode of a mold has the dark current, an after-image, a reset noise, a blooming, and the effectiveness of reducing a smear.

[0072] the 2nd P type for the perpendicular transfer register 220 to oppress the N type transfer channel field 221 and a smear noise, as shown in drawing 19 and drawing 20 -- a well -- it consists of transfer electrodes 223-225 formed in the field 222 and N type transfer channel field 221 upper part through the insulator layer 202. The above-mentioned transfer electrodes 223-225 constitute the register for one step (three-phase-circuit drive CCD) from three electrodes in the direction of a train, and the driving pulse phiV1 to phiV3 is impressed to each. That is, the transfer electrodes 223 and 225 which extend in a line writing direction, and the transfer electrode 224 which extends in the direction of a train are arranged, and the perpendicular transfer register for one step is prepared to one photodiode 210. Therefore, this solid state image sensor is the so-called CCD mold solid state image sensor of all pixel read-out methods.

[0073] The P type channel stopper 230 was formed in the perimeter of a photodiode 210, and has separated between the photodiodes 210 which adjoin between a photodiode 210 and the perpendicular transfer register 220 and in the direction of a train. The P type channel stopper 230 is not formed in the lower part of the transfer gate TG as shown in drawing 19 . Therefore, the signal charge generated with each photodiode 210 is accumulated in a photodiode 210, and when the transfer gate TG turns on, it is transmitted to the perpendicular transfer register 220 via the field of the lower part of the transfer gate TG. In drawing 19 - drawing 21 , the arrow head has shown the sense which a signal charge moves.

[0074] Moreover, as a light-shielding film 226 shows drawing 19 and drawing 20 , it is formed in the 223 to transfer electrode 225 upper part on a perpendicular transfer register through an insulator layer 202. The location where the transfer gate TG is arranged is reversed by the eventh line with the oddth line. However, the configuration of a light sensing portion becomes the same and a light-receiving property is equalized by the light-shielding film 226. In addition, the three-phase-circuit drive CCD was used for the perpendicular transfer register in this operation gestalt. However, not only this but 4 phase drives CCD are sufficient.

[0075] as mentioned above, the solid state image sensor of the operation gestalt 8 has been arranged in checkers -- green -- one level transfer register 240a is transmitted to the signal charge of the photodiode 210 equipped with the color filter of (G), it is changed into a voltage signal in one charge detecting-element 250a, and is outputted from one output terminal 260a. Therefore, while latter signal processing becomes easy, a fixed pattern noise decreases and a S/N ratio improves.

[0076] Moreover, the solid state image sensors of the operation gestalt 8 are the oddth line and the eventh line, since the cross-section configuration including the superficial configuration and wiring of a light-shielding film 226, or an insulator layer is the same, a fixed pattern noise decreases and its S/N ratio improves further. Moreover, since the photodiode 210 of a flush type is adopted with vertical mold overflow drain structure, the reset noise generated in the charge detecting elements 250a and 250b and a 1/f noise decrease by the dark current, an after-image, a reset noise and a blooming, and a smear decreasing, and carrying out the so-called correlation duplex sampling processing in the latter part of the charge detecting elements 250a and 250b. Therefore, a S/N ratio improves further.

[0077] Next, the system which processes the signal outputted from the solid state image sensor concerning this invention is explained. Drawing 22 is the block diagram showing an example of the signal processor which processes the signal outputted from the solid

state image sensor concerning this invention. The solid state image sensor concerning this invention outputs the signal from the remaining pixels outside for the signal from the pixel arranged in checkers from the signal terminal of another side from one output terminal like the above-mentioned explanation. And corresponding to the pixel arranged in checkers, it is suitable as a solid state image sensor for [which arranges a blue (B) color filter with red (R) to the color filter of (G), and other pixels line sequential (Bayer array)] colors green.

[0078] As mentioned above, this signal processor carries out a color image pick-up using the solid state image sensor of this invention with which the color filter has been arranged at each pixel, and returns the signal outputted to two terminals by the ability distributing to the time series signal corresponding to the location of a pixel. In the solid state image sensor of this invention shown in the operation gestalt 8 from the operation gestalt 1, the signal (G signal and R/B signal) of the pixel obtained from two output terminals is outputted with the same drive clock. Therefore, drive frequency is one half of the frequencies of the frequency of the scan clock (PIXCLK) decided by the number of pixels. Therefore, Rhine which is early outputted by 1 pixel by Rhine which is outputted to the timing which suited the pixel by the 1st channel when output timing horizontal on the basis of the scan head pixel of the 1st channel was seen, and is early outputted by 1 pixel by the 2nd channel, and the 1st channel, and is early outputted by 2 pixels by the 2nd channel will be arranged by turns.

[0079] As for this equipment, the 1st channel of the above and the line sequential signal of R and B are outputted for G signal as the 2nd channel. G signal is the same frequency as the signal output frequency of a solid state image sensor, and an AD translation is carried out to an output signal according to timing. An AD translation frequency is 1/2 of PIXCLK. Since G signal is the 1st channel output, it takes timing by DFF86 to which a change and both of the signals synchronized with PIXCLK corresponding to a pixel location the signal which does not shift timing horizontally, and the signal delayed by 1 pixel by DL82 (DFF to which the stereo synchronized with PIXCLK) for every Rhine by the change signal HMPX in MPX84, and is sent to the signal-processing section 89. In addition, it has sent the G-pixel signal each to the signal-processing section as magnitude for 2 pixels horizontally on account of signal processing. This inserts a black pixel (0 level signals) in the pixel by which the green (G) color filter is not arranged, and may be made to be outputted to it.

[0080] After signal processing of the 2nd channel by which B signal and R signal are outputted to line sequential is carried out like the 1st channel (G signal), it is delayed by 1 more pixel by DFF88, and is sent to the signal-processing section 89. The

signal-processing section 89 is the signal-processing section for Bayer arrays, performs signal processing, such as color separation of R/B, pixel interpolation of the vacancy of RGB each color, and gamma processing, and is outputted as an RGB code which has the chrominance signal of all RGB in all pixels.

[0081]

[Effect of the Invention] The solid state image sensor by this invention can reduce the fixed pattern noise of the signal outputted from the pixel or the photo-electric-conversion section arranged in checkers, and is effective in a S/N ratio improving as explained in full detail above. Moreover, if at least one kind of color filter is arranged to the solid state image sensor of this invention in checkers and a color video signal is made to output to it, it will become possible to acquire the color video signal with which the fixed pattern noise was reduced, and to acquire good image quality. Especially in case the color filter of such an array is used for the solid state image sensor of this invention, it is suitable.

[0082] Moreover, if the superficial configuration of a protection-from-light field is made the same for the solid state image sensor of this invention by the pixel (or photo-electric-conversion section) of the oddth line, and the pixel (or photo-electric-conversion section) of the eventh line, a fixed pattern noise decreases and it is effective in a S/N ratio improving. Furthermore, if the cross-section configuration of the whole pixel containing wiring, an insulator layer, etc. is also made the same, a fixed pattern noise will decrease further and a S/N ratio will improve further.

[0083] Moreover, if the output section is arranged to the pixel of the solid state image sensor of this invention, it will become possible to output the signal (for example, the signal by which charge magnification was carried out and the signal by which current amplification was carried out) changed by the charge produced in the photo-electric-conversion section. The signal charge accumulated in the output section is held until it is initialized. Therefore, it also becomes possible to read two or more times with such a configuration.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the circuit diagram showing the outline of the solid state image sensor by the operation gestalt 1 of this invention.

[Drawing 2] It is the circuit diagram showing the outline of the solid state image sensor by the operation gestalt 2 of this invention.

[Drawing 3] It is the circuit diagram of the solid state image sensor by the operation gestalt 3 of this invention.

[Drawing 4] It is the circuit diagram showing the configuration of the solid state image sensor by the operation gestalt 4 of this invention.

[Drawing 5] It is the top view of two or more pixels of the solid state image sensor concerning the operation gestalt 4.

[Drawing 6] It is the top view of one pixel of the solid state image sensor concerning the operation gestalt 4.

[Drawing 7] It is the sectional view which met X1-X2 line of drawing 6 .

[Drawing 8] It is the sectional view which met Y1-Y2 line of drawing 6 .

[Drawing 9] It is the sectional view which met Y3-Y4 line of drawing 6 .

[Drawing 10] It is the circuit diagram showing the configuration of the solid state image sensor by the operation gestalt 5 of this invention.

[Drawing 11] It is the top view of two or more pixels arranged in the shape of [of the solid state image sensor concerning the operation gestalt 5] a matrix. It is the top view of the solid state image sensor by the operation gestalt 5 of this invention.

[Drawing 12] It is the top view of one pixel of the solid state image sensor concerning the operation gestalt 5 of this invention.

[Drawing 13] It is the sectional view which met X1-X2 line of drawing 12 .

[Drawing 14] It is the sectional view which met Y1-Y2 line of drawing 12 .

[Drawing 15] It is the sectional view which met Y3-Y4 line of drawing 12 .

[Drawing 16] It is the top view of two or more pixels arranged in the shape of [of the solid state image sensor concerning the operation gestalt 6 of this invention] a matrix.

[Drawing 17] It is the circuit diagram showing the outline of the solid state image sensor by the operation gestalt 7 of this invention.
[Drawing 18] It is the block diagram showing the outline of the solid state image sensor by the operation gestalt 8 of this invention.
[Drawing 19] It is the top view of the field 300 surrounded with the broken line of drawing 18 .
[Drawing 20] It is the sectional view which met X1-X2 line of drawing 19 .
[Drawing 21] It is the sectional view which met X3-X4 line of drawing 19 .
[Drawing 22] It is the block diagram showing an example of the signal processor which processes the signal outputted from the solid state image sensor concerning this invention.
[Drawing 23] It is the circuit diagram showing the main configurations of the conventional X-Y address type solid state image sensor.
[Drawing 24] It is the top view of two or more pixels arranged in the shape of [of the conventional X-Y address type solid state image sensor] a matrix.
[Drawing 25] It is the outline block diagram of the conventional CCD mold solid state image sensor.
[Drawing 26] It is the sectional view of the CCD mold solid state image sensor which met X1-X2 line of drawing 25 .
[Drawing 27] It is drawing showing an example of a color filter array.
[Drawing 28] It is drawing showing other examples of a color filter array.
[Description of Notations]
1 Photodiode
2 JFET
3 Transfer Gate
4 Reset Drain
5 Reset Gate
6a Overflow control field
7 Vertical-Scanning Circuit
8 Horizontal Scanning Circuit
9a-9c Line selection line
10 P-type Semiconductor Substrate
11 N Type -- Well -- Field
12 P Type Charge Storage Field
13 High-concentration N-type Semiconductor Field
14 N Type Source Field

15 P Type Gate Field
16 N Type Drain Field
17 N Type Channel Field
18 P Type Charge Discharge Field
20, 20a-20c Transfer gate wiring
21, 21a-21c Reset gate wiring
22, 22a-22d Perpendicular signal line
23 Junction Wiring
24, 24a-24c Reset drain wiring
26a-26d Constant current source
27a-27d Level signal line
28a-28d Output-buffer amplifier
29a-29d Train buffer amplifier
33 Insulator Layer
34a, 34b Differential amplifier
35a, 35b Output terminal
41 Photodiode
42 Line Selection Transistor
51 Photodiode
52 Output Transistor
53 Reset Transistor
54 Line Selection Transistor
55a-55c Reset gate wiring
56a-56c Line selection line
80 81 A-D converter
82 83 Delay element
84 85 Multiplexer
86, 87, 88 D flip-flop
89 Signal-Processing Section for Bayer Arrays
100 High-concentration N-type Semiconductor Substrate
101 N-type Semiconductor Layer
200 N-type Semiconductor Substrate
201 P Type -- Well -- Field
202 Insulator Layer
210 Photodiode
211 N Type Charge Storage Field

212 High-concentration P-type Semiconductor Field
220 Perpendicular Transfer Register
221 N Type Transfer Channel Field
222 2nd P Type -- Well -- Field
223,224,225 Transfer electrode
226 Light-shielding Film
230 P Type Channel Stopper
240a, 240b Level transfer register
250a, 250b Charge detecting element
260a, 260b Output terminal